HIGH EFFICIENCY SUBMICRON GATE LDMOS POWER FET FOR LOW VOLTAGE WIRELESS COMMUNICATIONS

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ABSTRACT

A low cost, high efficiency silicon MOSFET using 0.6µm LDMOS (LV3) technology was developed in Motorola for high frequency (1-2 GHz) and low voltage (3.4-12.5V) wireless applications. The LV3 devices can deliver 77% power added efficiency (PAE) with 12 dB gain, 28.7 dBm output power at 3.4V and 850 MHz. The LV3 devices also can provide 70% PAE, 11 dB gain, 36 dBm Pout at 6V, 850 MHz and 50% PAE, 9 dB gain, 33 dBm Pout at 5.8V, 1.9 GHz. This is the best known RF performance for silicon devices at 3.4V and 6V.

INTRDUCTION

Higher efficiency RF power devices operating at lower voltages are required to reduce the battery size, weight and power consumption and increase talk time for new generation portable communication products. A low cost, high efficiency 3rd generation silicon MOSFET using RFLDMOS [LV3] 0.6 µm technology was developed in Motorola to operate at low drain voltages. Various techniques such as channel and drain engineering, layout and process optimization have been implemented to improve LDMOS device efficiency at high frequency and low voltages. This paper will focus on the techniques used to enhance LV3 devices performance. The results of LV3 devices for various applications will also be presented.

DEVICE DESIGN

The cross-section of a low voltage RFLDMOS transistor is shown on Fig. 1. The device is fabricated on a p+ substrate, on which a p- epi layer (10 Ωcm) is grown. A p+ sinker implant is used to connect the topside source to the backside metal contact. A 400Å gate oxide is grown to sustain Vgs stress up to 12V. An 1.2 Ω/square silicide gate is employed to provide a superior RF power gain. The device has a laterally diffused channel implant (p-type) which controls the threshold voltage and provides a higher device transconductance (gm) than a standard NMOS device. A lightly doped n- region is used to reduce the electric field in the drain side. The dose and drift length of the n- drain region can be tailored to optimize device Rdson, BVdss and drain to gate capacitance (Cdg). The device also includes a metal field plate which overlaps the gate and is connected to the source. This gate plate reduces the fields at the edge of the gate thus increasing the breakdown voltage and reducing Cdg.

The critical device design parameters for efficiency and gain improvement are device on resistance, capacitances, transconductance, and layout configuration (phase balance between gate fingers and thermal balance between unit cells). The Cgs and Cgd reduction was realized by shrinking the gate length from 1 µm (LV2) to 0.6 µm (LV3). The Cgd was further reduced by removing the nitride layer in the dielectric stack (ILD) and reducing the polygate height from 5000Å to 2000Å. A double HIPOX process was employed to planarize the surface and increase the field oxide thickness from 1.9 µm (LV2) to 2.4 µm (LV3), thus reducing the Cgs and Cds. The channel doping profile was optimized by implementing a higher dose channel implant followed by a shorter drive to suppress the short channel effect while increasing the device transconductance. The device safe operating region was established by N-, P-Ch doses and BVdss optimization (Fig. 2). Various other process and device optimization techniques have also been investigated. Table 1 shows the LV3 device and process optimization summary. Various layout configurations with different active area aspect

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ratio were employed in a test mask set to optimize the phase balance between gate fingers and the thermal balance between unit cells. The 42 fingers per cell layout option was chosen as the baseline LV3 device structure (Fig. 3).

RESULTS

The LV3 and LV2 DC parameters are comparable. However, the LV3 capacitance Cgs, Cgd, Cds show 11%, 50%, 5% reduction compared to the LV2 device respectively. The LV3 devices can deliver 77% PAE with 12 dB gain, 28.7 dBm output power at 3.4V and 850 MHz (Fig. 4). The LV3 devices also can provide 70% PAE, 11 dB gain, 36 dBm Pout at 6V, 850 MHz for GSM application (Fig. 5). For the PCS and DCS applications, the LV3 devices show 50% PAE, 9 dB gain, 33 dBm Pout at 5.8V, 1.9 GHz (Fig. 6). The LV3 technology can also be used for higher voltage applications (6-12.5V) by adjusting the N- drift length to meet the BVdss requirements.

CONCLUSION

In summary, the LV3 device provides a low cost, single power supply, high efficiency solution for wireless communications operating at high frequency and low voltages. Further device, process, layout, and substrate/epi material optimization (LV4) are in progress in Motorola to enhance LDMOS performance.

ACKNOWLEDGEMENTS

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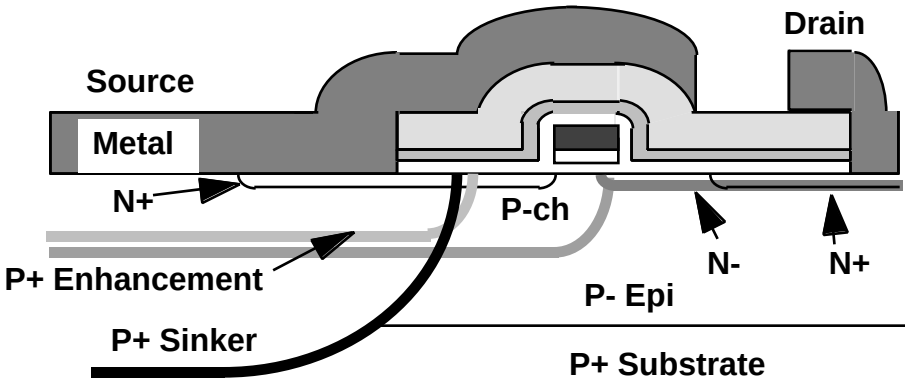

Fig. 1 RFLDMOS device cross section

Paramete	Cap	Ruggednes	PAE/Gai
Field Oxide 1.9 => 2.4	+		+
Gate Length 1. => 0.6	++	-	++
P-CH Dose 1.9 => 3.3	-	++	
N- Dose 2.0E12 =>	-	- -	+
P-CH Drive	+	-	+
Polygate thk 5000 Å =>	+		+
Nitride	+		+
56 Finger => 42 Finger	-		++

"++" = large
" - -" = large

Table 1 LV3 device

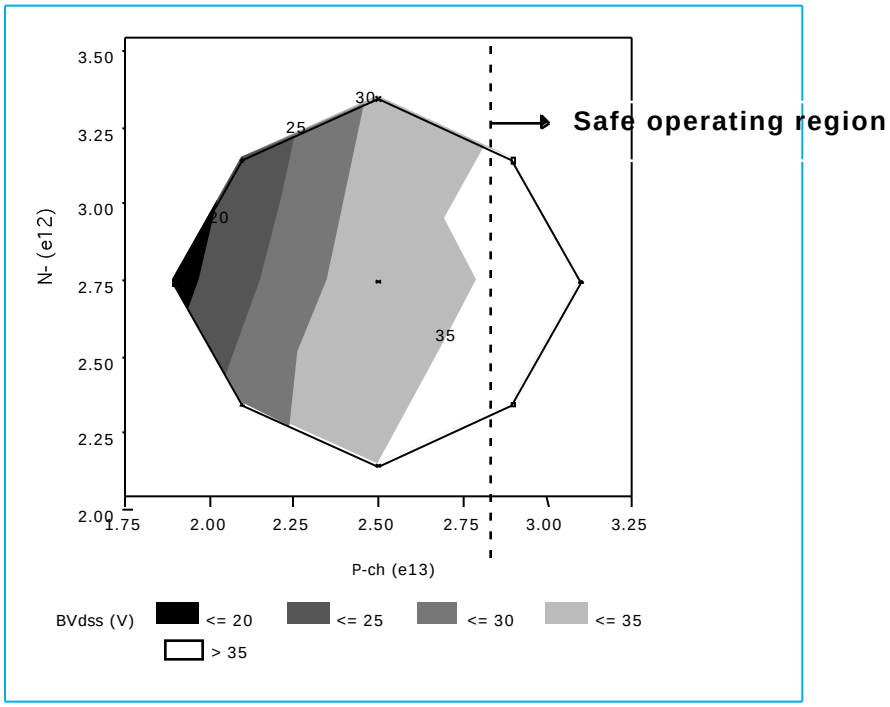

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Fig. 2 N- and P-ch doses vs BVdss optimization. BVdss does not depend on N- and P-ch does in the safe operating region.

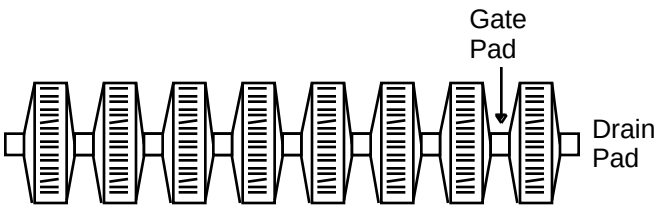

Fig. 3 The 42 fingers per cell LV3 configuration.

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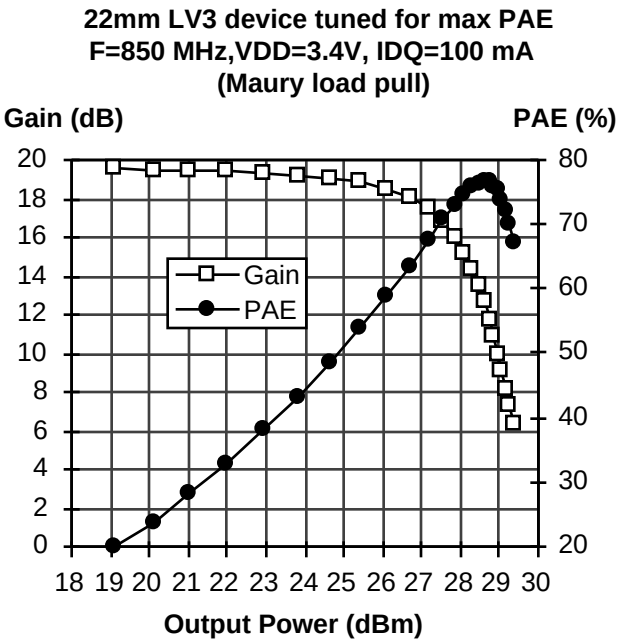

Fig. 4 LV3 device gain & power added efficiency vs output power for 3.4V applications

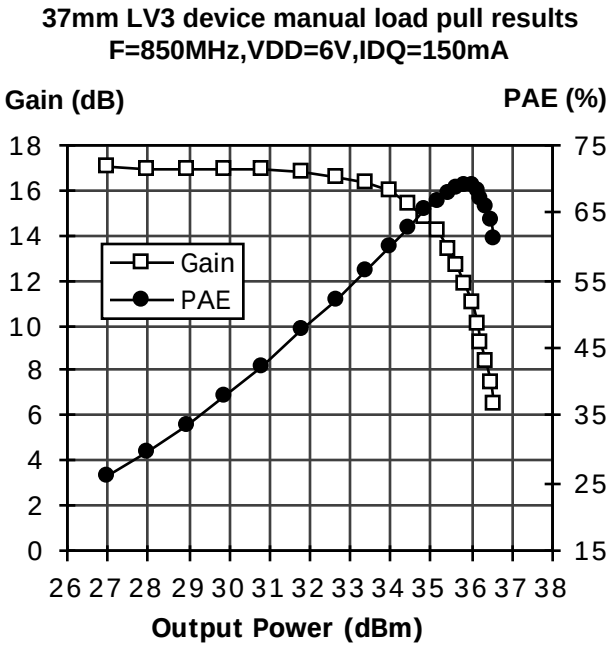

Fig. 5 LV3 device gain & power added efficiency vs output power for 6V GSM application

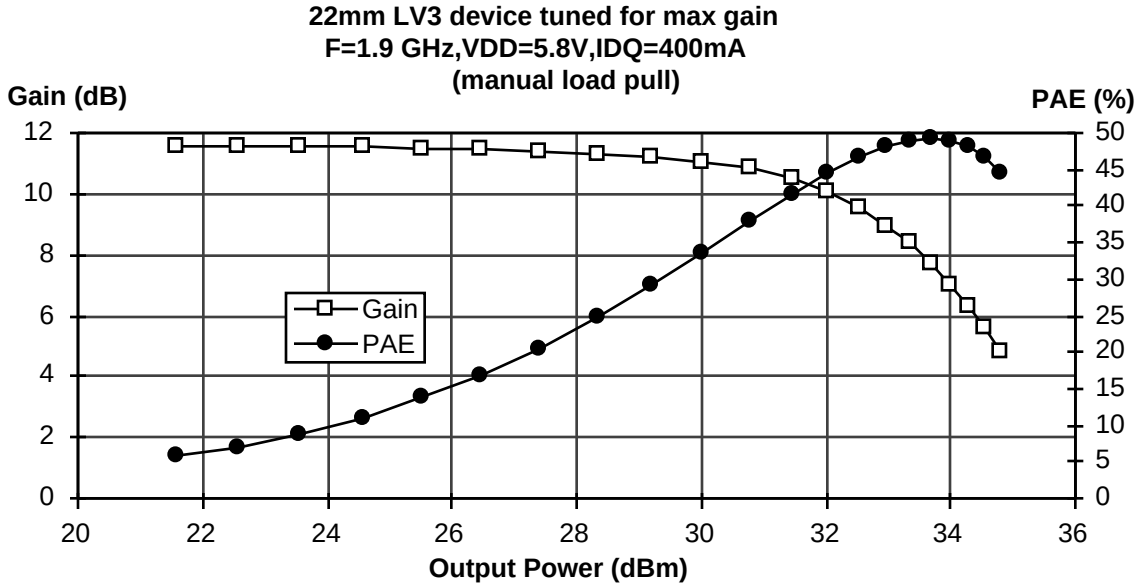

Fig. 6 LV3 device gain & power added efficiency vs output power for 2 GHz applications.